SHADER PIXEL STORAGE IN A GRAPHICS MEMORY

ABSTRACT

Circuits, apparatus, and methods that enable a shader to read and write data from and to a memory location during a single pass through a graphics pipeline. Some embodiments of the present invention provide an increase in the number of buffers available to a shader. These buffers may be read/write (input/output) or read only (input) buffers. Another provides pixel store and pixel load commands that may be used as instructions in a shader program or program portion, and may appear at positions other than the end of the shader program or program portion. Other embodiments provide a data path between a shader and a graphics memory, typically through a frame buffer interface. This data path simplifies the timing of the above store (write) and load (read) commands. Various embodiments may incorporate one or more of these features.